Serie 11 - Solution

Given constants

$kT/q = 25.9\,[mV] \quad @ \quad T = 300\,[K]$
$n_i(Si) = 1.5 \cdot 10^{10}\,[cm^{-3}] \quad @ \quad T = 300\,[K]$
$q = 1.60 \cdot 10^{-19}\,[C]$
$\epsilon_0 = 8.85 \cdot 10^{-14}\,[F/cm]$
$\epsilon_{Si} = 11.7 \cdot \epsilon_0$
$\epsilon_{SiO} = 3.9 \cdot \epsilon_0$

Exercise 01

You have access to the specifications of an industrial CMOS technology that we want to consider for the design of an IC operating at $T = 85\,[°C]$. For a long-channel NMOS transistor, we have: an off current $I_{off} = 1\,[nA/\mu m]$, a threshold voltage $V_{th} = 0.5\,[V]$, a subthreshold slope $SS = 70\,[mV/dec]$, all at $T = 25\,[°C]$. The current I_{off} is the current I_D at $V_{GS} = 0\,[V]$ and $V_{DS} = V_{DD}$, normalized by the channel width W. The subthreshold slope is defined as $SS = \frac{\partial V_{GS}}{\partial(log_{10} I_D)} = ln(10) \cdot \frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right)$ (in subthreshold, of course). The following formula holds:

$$I_D(V_{th}) = I_{off} \cdot 10^{\frac{V_{th}}{SS}}$$

Extract I_{off} at $T = 85\,[°C]$. Assume that the threshold voltage of your MOSFET changes with temperature according to $\frac{dV_{th}}{dT} = -4\,[mV/°C]$, over the range of interest for your application. Hint: exploit the fact that the current $I_D(V_{th})$ is defined constant, independently of V_{th}.

Solution

We start by calculating the current $I_D(V_{th})$ at threshold by using the formula above, since we know the I_{off}, V_{th} and SS at $T = 25\,[°C]$:

$$I_D(V_{th}) = I_{off} \cdot 10^{\frac{V_{th}}{SS}} \approx 13.9\,[mA/\mu m] \tag{1}$$

We fix this current value as the current at threshold, independently of the temperature, i.e. $I_D(V_{th\ @25[°C]}) = I_D(V_{th\ @85[°C]}) \approx 13.9\,[mA/\mu m]$.
Now, we can retrieve I_{off} at $T = 85\,[°C]$ by using the same formula. We just need to substitute V_{th} and SS with their respective values at $T = 85\,[°C]$.
Let's calculate the threshold shift ΔV_{th} between $25\,[°C]$ and $85\,[°C]$:

$$\Delta V_{th} = \frac{\partial V_{th}}{\partial T}\Delta T = -\frac{4\,[mV]}{[°C]} \cdot 60\,[°C] = -240\,[mV] \tag{2}$$

so that:

$$V_{th\ @85[^\circ C]} = V_{th\ @25[^\circ C]} - \Delta V_{th} = 260\,[mV] \tag{3}$$

To calculate the SS at $85\,[^\circ C]$, let's convert the two temperatures to $[K]$:

$$T_1 = 25\,[^\circ C] = (25{+}273)\,[K] = 298\,[K] \quad , \quad T_2 = 85\,[^\circ C] = (85{+}273)\,[K] = 358\,[K]$$

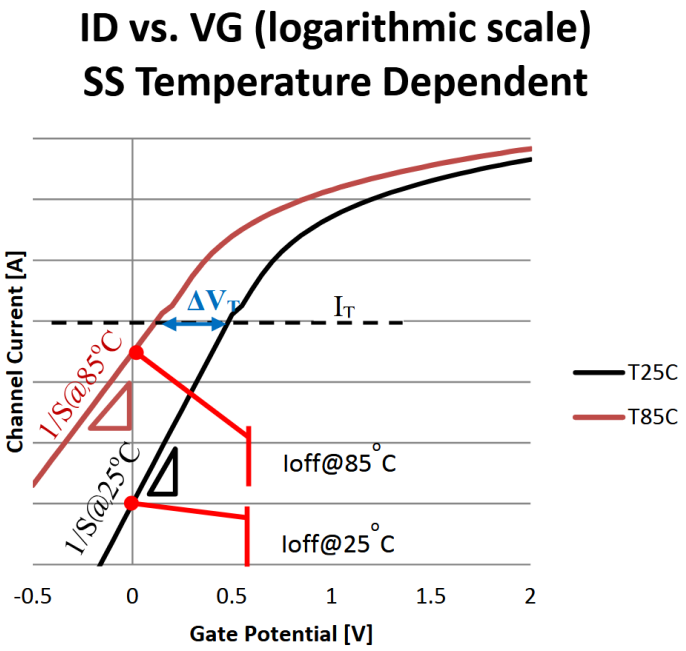
and apply the following proportionality, that comes from the definition of SS:

$$SS_{@358[K]} = SS_{@298[K]} \cdot \frac{358\,[K]}{298\,[K]} \approx 84\,[mV/dec] \tag{4}$$

We finally calculate I_{off} at $T = 85\,[^\circ C]$:

$$\begin{aligned} I_{off\ @85[^\circ C]} &= I_D(V_{th}) \cdot 10^{-\frac{V_{th\ @85[^\circ C]}}{SS_{@85[^\circ C]}}} = \\ &= 13.9\,[mA/\mu m] \cdot 10^{-\frac{260[mV]}{84[mV/dec]}} \approx 11.2\,[\mu A/\mu m] \end{aligned} \tag{5}$$

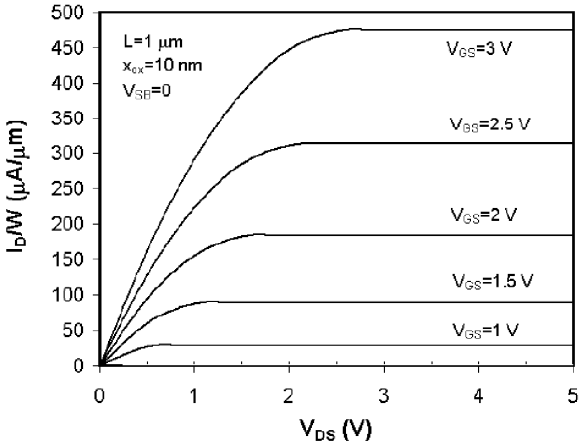
which is 10^4 times higher than $I_{off\ @25[^\circ C]}$.
A schematic plot of what happens to the MOSFET transcharacteristic by increasing the temperature is reported below. You can clearly see the two effects calculated in this exercise: the threshold voltage shift and the subthreshold slope increase, that result in an increase in the off current.
(I_T is the fixed value we called $I_D(V_{th})$)



Exercise 02

Consider the output characteristic $I_D(V_D)$ (reported below) of a long-channel NMOS transistor, for the case where its body contact (B) is shorted with the source (S) to ground ($0\,[V]$). The channel length is $L = 1\,[\mu m]$ and the gate oxide thickness is $t_{ox} = 10\,[nm]$. Answer the following questions:

- Assuming that the MOSFET has quasi-ideal long-channel transistor behavior, estimate its threshold voltage V_{th}.
- Estimate the electron mobility μ_n of its inversion channel at low transverse field. How does this value compare with the volume electron mobility?
- Estimate its transconductance g_m at $V_{GS} = 3\,[V]$ and $V_{DS} = 3\,[V]$ for $W = 10\,[\mu m]$, under the same assumption of the first point. Comment on the possibility of choosing the transconductance value by design and compare it with the value of a bipolar transistor.
- Estimate the capacitance C_{GS} for the same V_{GS}, V_{DS} and W. In saturation: $C_{GS} \approx \frac{2}{3} W L C_{ox}$.



Solution

We know that $V_{DSsat} = V_{GS} - V_{th}$ and we can easily estimate V_{DSsat} as a function of V_{GS} from the plot:

V_{GS} (V)	1	1.5	2	2.5	3
V_{DSsat} (V)	0.5	1	1.5	2	2.5

Therefore, $V_{th} = V_{GS} - V_{DSsat} = 0.5\,[V]$.
We can estimate the electron mobility μ_n from the formula for the current I_D in saturation (and strong inversion). We can neglect channel length modulation since the MOSFET in this exercise behaves as a quasi-ideal long-channel transistor. We write:

$$I_D = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_{th})^2 \quad \Leftrightarrow \quad \mu_n = \frac{I_D}{W}\frac{2L}{C_{ox}(V_{GS} - V_{th})^2} \tag{6}$$

Let's extract I_D/W in saturation as a function of V_{GS} from the plot:

I_{DSsat}/W (µA/µm)	25	75	175	300	475
V_{GS} (V)	1	1.5	2	2.5	3

The oxide capacitance (SiO_2) is:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 3.45 \cdot 10^{-7}\,\left[F/cm^2\right] \tag{7}$$

We are asked to find the electron mobility at low transversal field, thus we will consider the saturation current for the lowest value of $V_{GS} = 1\,[V]$, i.e. $I_D/W = 25\,[\mu A/\mu m] = 0.25\,[A/cm]$. Then, we can calculate:

$$\mu_n = \frac{I_D}{W}\frac{2L}{C_{ox}(V_{GS} - V_{th})^2} = 579.7\,\left[cm^2V^{-1}s^{-1}\right] \tag{8}$$

This value is lower than the bulk electron mobility, which is in the order of $1000 - 1350\,\left[cm^2V^{-1}s^{-1}\right]$ in lightly doped Si at low field at $300\,[K]$. This is due to the Si/SiO_2 surface effects that carriers in the channel undergo, in addition to the bulk scattering mechanisms.
Now we need to calculate the transconductance at $V_{GS} = 3\,[V]$ and $V_{DS} = 3\,[V]$. Since $V_{GS} > V_{th}$ and $V_{DS} > V_{GS} - V_{th}$, we are in strong inversion and saturation, for which:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th}) \tag{9}$$

We know $W = 10\,[\mu m]$. The beta-factor $\beta = \mu_n C_{ox}\frac{W}{L}$ can be extracted from the plot as follows:

$$\frac{I_D}{W} = \frac{1}{2L}\mu_n C_{ox}(V_{GS} - V_{th})^2 \quad \Leftrightarrow \quad \mu_n C_{ox}\frac{W}{L} = \frac{I_D}{W}\frac{2W}{(V_{GS} - V_{th})^2} = \\ = 1.52 \cdot 10^{-3}\,\left[A/V^2\right] \tag{10}$$

Consequently:

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th}) = 3.8\,[mS] \tag{11}$$

In a MOSFET, the transconductance value can be tuned by adjusting the design parameters W and L. We recall that the transconductance formula for the BJT is:

$$g_m = \frac{\partial i_c}{\partial v_{BE}} = \frac{qI_c}{kT} \tag{12}$$

If we suppose the same current value $I_c/W = 475\,[\mu A/\mu m]$, as the one of this MOSFET, the transconductance of the BJT at $300\,[K]$ is $g_m = 183.4\,[mS]$, which is almost 10^2 times higher than that of the MOSFET.
For the last point, we have to calculate the capacitance C_{GS} at the same operating point.

Explanation on MOSFET C_{GS} and C_{GD} capacitances

We report in the Figure below the behavior of the capacitances C_{GS} and C_{GD} as a function of the gate voltage V_{GS}. As you can see, the two capacitances are the sum of two contributions: 1) a fixed term $W x_{ov} C_{ox}$ given by the overlaps between the source/drain and the gate terminal, that do not depend on the operating region and are set by design; 2) a variable term given by the inversion charge along the channel length, that indeed depends on the operating region. This second term is negligible in weak inversion ($V_{GS} < V_{th}$) for both C_{GS} and C_{GD}. It is approximately equal to $W\frac{L}{2}C_{ox}$ in strong inversion and triode for both C_{GS} and C_{GD}, since the channel is almost uniformly charged. Instead, it is negligible for C_{GD} and around $W\frac{2L}{3}C_{ox}$ for C_{GS} in strong inversion and saturation. The difference between the two contributions in saturation is due to the channel pinch-off: the inversion channel is present close to the source while a depletion region is formed between the pinch-off point and the drain.
If we consider a long-channel transistor, the overlap between source/drain and the gate will be $x_{ov} << L$. Therefore we can approximate quite accurately the source-gate capacitance in saturation as:

$$C_{GS} = W\left(x_{ov} + \frac{2L}{3}\right)C_{ox} \approx W\frac{2L}{3}C_{ox} = 2.3 \cdot 10^{-14}\,[F] \tag{13}$$

Proof:

We assume the transistor has a long channel, so that $x_{ov} << L$, and the contribution due to the overlap between Source/Drain and Gate can be neglected. At the onset of saturation ($V_{DS} = V_{GS} - V_{th}$), the current is given by:

$$I_D = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_{th})^2 \tag{14}$$

Assume an arbitrary point X along the channel which lays between $x = 0$ (Source) and $x = L$ (Drain), where $x = X$. Consider the part of device between Source and X as a MOSFET on its own. V_{XS} will be the potential difference over its partial channel and I_X will be its current. This part of the channel will be in linear operation as $V_{XS} < V_{DS} = V_{GS} - V_{th}$, therefore its current will be:

$$I_X = \frac{W}{X}\mu_n C_{ox}\left(V_{GS} - V_{th} - \frac{V_{XS}}{2}\right)V_{XS} \tag{15}$$

But in fact I_X and I_D are equal:

$$\begin{aligned}
I_D = I_X \quad &\Leftrightarrow \quad \frac{W}{2L}\mu_n C_{ox}(V_{GS}-V_{th})^2 = \frac{W}{X}\mu_n C_{ox}\left(V_{GS}-V_{th}-\frac{V_{XS}}{2}\right)V_{XS} \\
&\Leftrightarrow \quad \frac{(V_{GS}-V_{th})^2}{2L} = \frac{\left(V_{GS}-V_{th}-\frac{V_{XS}}{2}\right)V_{XS}}{X} \\
&\Leftrightarrow \quad \frac{(V_{GS}-V_{th})^2}{L} = \frac{2(V_{GS}-V_{th})V_{XS}-V_{XS}^2}{X} \\
&\Leftrightarrow \quad \frac{(V_{GS}-V_{th})^2}{L} = \frac{(V_{GS}-V_{th})^2-(V_{GS}-V_{th})^2+2(V_{GS}-V_{th})V_{XS}-V_{XS}^2}{X} \\
&\Leftrightarrow \quad \frac{(V_{GS}-V_{th})^2}{L} = \frac{(V_{GS}-V_{th})^2-(V_{GS}-V_{th}-V_{XS})^2}{X} \\
&\Leftrightarrow \quad \frac{X}{L}(V_{GS}-V_{th})^2-(V_{GS}-V_{th})^2 = -(V_{GS}-V_{th}-V_{XS})^2 \\
&\Leftrightarrow \quad (V_{GS}-V_{th})^2\left(1-\frac{X}{L}\right) = (V_{GS}-V_{th}-V_{XS})^2 \\
&\Leftrightarrow \quad V_{GS}-V_{th}-V_{XS} = (V_{GS}-V_{th})\sqrt{1-\frac{X}{L}} \\
&\Leftrightarrow \quad V_{XS} = (V_{GS}-V_{th})\left(1-\sqrt{1-\frac{X}{L}}\right)
\end{aligned} \tag{16}$$

The above equation gives the potential at any point inside the channel with respect to its position, when the MOSFET is at the onset of saturation. The inversion charge at each point X of the channel (where the potential is V_{XS}) is given by:

$$Q_i(x) = -WC_{ox}(V_{GS}-V_{th}-V_{XS}) = -WC_{ox}(V_{GS}-V_{th})\sqrt{1-\frac{X}{L}} \tag{17}$$

The total inversion charge is:

$$\begin{aligned}
Q_{I,total} &= \int_0^L Q_i(x)\,dx = \int_0^L -WC_{ox}(V_{GS}-V_{th})\sqrt{1-\frac{X}{L}}\,dx = \\
&= -WC_{ox}(V_{GS}-V_{th})\int_0^L \sqrt{1-\frac{X}{L}}\,dx = \\
&= -WC_{ox}(V_{GS}-V_{th})\left[-\frac{2L}{3}\left(1-\frac{X}{L}\right)^{\frac{3}{2}}\right]_0^L = \\
&= -\frac{2}{3}WLC_{ox}(V_{GS}-V_{th})
\end{aligned} \tag{18}$$

The charge at the gate will be equal and opposite in sign to the total inversion charge at the channel:

$$Q_G = -Q_{I,total} = \frac{2}{3}WLC_{ox}(V_{GS}-V_{th}) \tag{19}$$

So:

$$C_{GS} = -\frac{dQ_G}{dV_S} = \frac{2}{3}WLC_{ox} = 2.3 \cdot 10^{-14}\,[F] \quad , \quad C_{GD} = -\frac{dQ_G}{dV_D} = 0 \qquad (20)$$

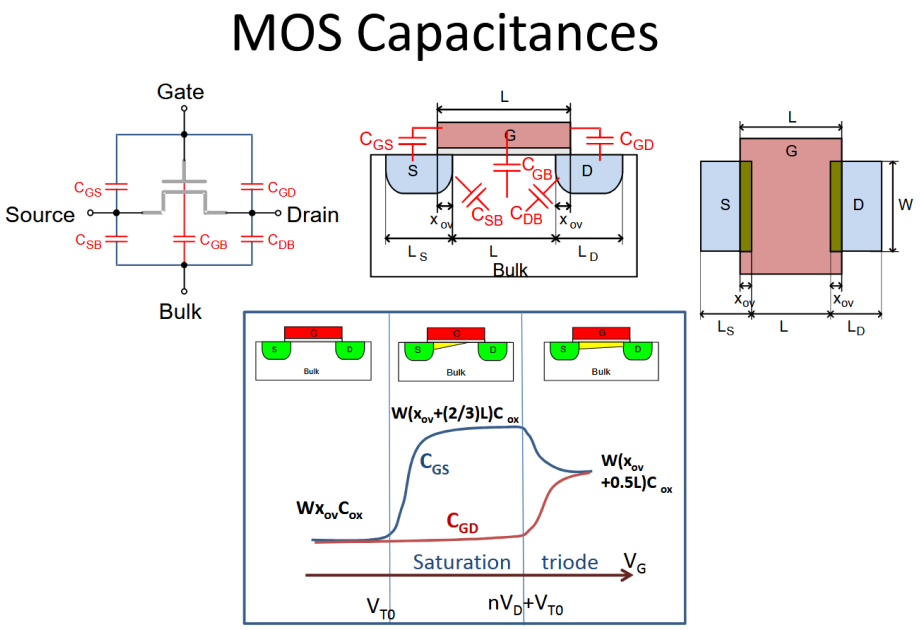


Figure 1: C_{GS} and C_{GD} of a MOSFET as a function of the gate voltage V_{GS}. Figure reported from the course "Analog circuit design II" by Professor A. Koukab, at EPFL.